IN THE CLAIMS:

Please amend the claims as follows:

1. (currently amended) A re-multiplexer module for transmitting a plurality of output data streams from a plurality of input data streams, comprising:

an input processing portion that receives a plurality of input data streams containing data packets;

a plurality of packet buffers for storing data packets of said input streams;

an output processing portion that selectively multiplexes data packets from said plurality of buffers to generate at least two output data streams; and

a host processor that controls the operation of the input processing portion and the output processing portion,

wherein said module also extracts messages from said input data streams and selectively adds messages to any of said at least two output data streams.

2. (original) The re-multiplexer module of claim 1, wherein the input processing portion includes a plurality of input interfaces and a plurality of input processors, each input interface receiving one of said plurality of input data streams and sending the input data stream to one of said plurality of input processors.

3. (original) The re-multiplexer module of claim 1, wherein the input processing portion includes a plurality of packet identifier tables, each packet identifier table coupled to one of said input processors.

4. (original) The re-multiplexer module of claim 3, wherein the packet identifier table includes an active table and a pending table, wherein the pending table can be modified while the input processing portion is operating from the active table.

5. (original) The re-multiplexer module of claim 4, wherein the packet identifier table includes a switching mechanism that allows the host processor to switch the

active table into a current pending table and switch the pending table into a current active table.

6. (original) The re-multiplexer module of claim 3, wherein each input interface has a corresponding packet identifier table.

7. (original) The re-multiplexer module of claim 1, wherein the packet buffer includes an input packet buffer that holds data from accepted packets in the input stream and an insert packet buffer that holds packet data that is to be inserted into the output stream.

8. (original) The re-multiplexer module of claim 1, wherein the output processing portion includes an output processor having a bus control logic block that controls the manner in which packets are read from the plurality of packet buffers.

9. (original) The re-multiplexer module of claim 8, wherein the output processing portion further comprises a message extraction portion that extracts selected messages from any of the plurality of the packet buffers.

10. (original) The re-multiplexer module of claim 9, wherein the message extraction portion includes a control message processor that extracts messages from the output stream and a extract message buffer that stores the extracted messages.

11. (original) The re-multiplexer module of claim 1, further comprising a system interface coupled to the output processing portion for linking the re-multiplexer module with other modules in a packet processing system.

12. (original) The re-multiplexer module of claim 1, wherein the output processing section further comprises an interface coupled to the output processor for outputting the output data streams.

13. (original) The re-multiplexer module of claim 12, wherein the interface includes at least one output interface to other modules in a packet processing system and a external equipment interface that acts as an output interface to devices outside of the packet processing system.

14. (original) The re-multiplexer module of claim 13, wherein an output interface and a external equipment interface is provided for each output data stream.

15. (currently amended) A re-multiplexer module for transmitting a plurality of output data streams from a plurality of input data streams, the re-multiplexer module being configured for use in a packet processing system, comprising:

an input processing portion that receives a plurality of input data streams containing data packets, the input processing portion having a plurality of input interfaces, a plurality of input processors, and a plurality of packet identifier tables, each input interface and packet identifier table corresponding with one of said plurality of input streams;

a plurality of packet buffers for storing data packets of said input streams, each packet buffer receiving an input from one of said plurality of input processors;

an output processing portion that selectively multiplexes data packets from said plurality of buffers to generate at least two output data streams, the output processing portion having at least two output interfaces ~~that act as an output interface to other modules in the MPS~~; and

a host processor that controls the operation of the input processing portion and the output processing portion.

16. (original) The re-multiplexer module of claim 15, wherein the input processing portion includes a plurality of packet identifier tables, each packet identifier table coupled to one of said plurality of input processors.

17. (original) The re-multiplexer module of claim 16, wherein the packet identifier table includes an active table and a pending table, wherein the pending table can be modified while the input processing portion is operating from the active table.

18. (original) The re-multiplexer module of claim 17, wherein the packet identifier includes a switching mechanism allowing the host processor to switch the active table into a current pending table and switch the pending table into a current active table.

19. (original) The re-multiplexer module of claim 15, wherein the packet buffer includes an input packet buffer portion that holds packet data from accepted packets in the input stream and an insert packet buffer portion that holds packet data that is to be inserted into the output data stream.

20. (original) The re-multiplexer module of claim 15, wherein the output processing portion includes an output processor having a bus control logic block that controls the manner in which packets are read from the plurality of packet buffers.

21. (original) The re-multiplexer module of claim 20, wherein the output processing portion further comprises a message extraction portion that extracts selected messages from the output stream generated by the output processor.

22. (original) The re-multiplexer module of claim 21, wherein the message extraction portion includes a control message processor that extracts messages from the output stream and a extract message buffer that stores the extracted messages.

23. (original) The re-multiplexer module of claim 15, further comprising a system interface coupled to the output processing portion for linking the re-multiplexer module with other modules in a packet processing system.

24. (original) The re-multiplexer module of claim 15, wherein the output processing section further comprises an output interface coupled to the output processor for outputting the output data streams.

25. (original) The re-multiplexer module of claim 24, wherein the interface includes at least one output interface that acts as an output interface to other modules in a packet processing system and a external equipment interface that acts as an output interface to

devices outside of the packet processing system, and wherein one output interface and one external equipment interface is provided for each output data stream.

26. (new) The re-multiplexer module of claim 1, wherein said module assigns new Packet Identifiers (PIDs) to packets taken from one of said input data streams and added to one of said output data streams.

27. (new) The re-multiplexer module of claim 1, wherein said input processing portion flags data packets having valid program clock reference (PCR) data.

28. (new) The re-multiplexer module of claim 27, wherein said output processing portion extracts said PCR data from said flagged data packets.

29. (new) The re-multiplexer module of claim 1, wherein said module has a priority mode in which packets having a set priority bit will be indicated as having a high priority than other valid packets and will be passed through the module before non-priority packets.

30. (new) The re-multiplexer module of claim 1, wherein said messages comprise either Program Association Tables (PATs) or Program Mat Tables (PMTs).

31. (new) The-multiplexer module of claim 15, wherein said module also extracts messages from said input data streams and selectively adds messages to said at least two output data streams.

32. (new) The re-multiplexer module of claim 15, wherein said module assigns new Packet Identifiers (PIDs) to packets taken from one of said input data streams and added to one of said output data streams.

33. (new) The re-multiplexer module of claim 15, wherein said input processing portion flags data packets having valid program clock reference (PCR) data.

34. (new) The re-multiplexer module of claim 33, wherein said output processing portion extracts said PCR data from said flagged data packets.

35. (new) The re-multiplexer module of claim 15, wherein said module has a priority mode in which packets having a set priority bit will be indicated as having a high priority than other valid packets and will be passed through the module before non-priority packets.

36. (new) The re-multiplexer module of claim 31, wherein said messages comprise either Program Association Tables (PATs) or Program Mat Tables (PMTs).

37. (new) A method of operating a re-multiplexer module to transmit a plurality of output data streams from a plurality of input data streams, comprising:

receiving a plurality of input data streams containing data packets;

storing data packets of said input streams;

selectively multiplexing stored data packets to generate at least two output data streams; and

extracting messages from said input data streams and selectively adding messages to any of said at least two output data streams.